DETAILED ACTION

Pñority

1. An application in which the benefits of an earlier, application are desired must contain a specific reference to the prior application(s) in the first sentence(s) of the specification or in an application data sheet by identifying the prior application by application number (37 CFR 1.78(a)(2) and (a)(5)).

When the nonprovisional application is entitled to an earlier U.S. effective filling date of one or more provisional application under *35* U.S.C. 119(e), a statement such as "This application claims the benefit of U.S. Provisional Application No. *06/245,942,* filed 11/06/2000." should appear as the first sentence of the description or in an application data sheet.

Reply to the Examiner's Comments

The specification has been amended to include claiming priority from the provisional application SN 60/245,942.

Drawings

Comments of the Examiner

The drawings are objected to as failing to comply with 37 CFR l.84(p)(4) because reference character "210" (Fig. 2) has been used to designate both upper and lower portions of a transistor. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immedi~te prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Reply to the Examiner's Comments

The reference character 210 on the top of the structure pointing to the MOS gate is a typographical error, this should be the same gate 204, since this gate is annual in shape and surrounds the source 209. A new corrected drawing is enclosed.

Claim Objections

Comments of the Examiner under the Rejection

Claims 1 & 7 are objected to because each of these claims recites, "said transistor having a gate surrounding its source and connected to it" which should be changed to --said vertical punch-through transistor having the gate surrounding the source and connected to the source--for proper antecedent basis.

Reply to the Examiner's Comments

In Claims 1 & 7, the wording has been changed to --- said vertical punch-through transistor having the gate surrounding the source and being conductively connected to the source---.

Claims 2, 3, 8 & 9 are also objected to because each of these claims recites, "the vertical charge-sensing punch-through transistor." The "charge-sensing" should be removed for proper antecedent basis.

Reply to the Examiner's Comments

In Claims 2,3,8 & 9: the "charge-sensing" word has been removed from the claims.

Comments of the Examiner

Claims 10-12 are also objected to because each of these claims recites, "the charge reset means" which is ONLY supported by claim 9,not claim 8. The Examiner suggests the Applicant to change dependency of each of claims 10-12 from claim 8 to claim 9 for proper antecedent basis.

Appropriate correction is required.

Reply to the Examiner's Comments

The dependency of Claims 10-12 has been changed from "8" to -9-.

Claim Rejections -35 USC §112

Claims 7-12 have been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Comments of the Examiner

Regarding independent claim 7, the claim recites "a CCD and CMOS device" which is not described in the specification as a single device.

Regarding claims 8-12, these claims are rejected as being dependent of claim 7.

The following rejection(s) applied to claims 7-12 based on best understood (by assuming BCD is a CCD and CMOS device) in view of the 112 first paragraph rejection above.

Reply to the Examiner's Comments

Claim 7 has been amended to Claim a CMOS device, and new Claims 13, 14, 15 and 16 have been added to claim a CCD device.

Claim Rejections -35 USC §112

Claims 4 & 10 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Comments of the Examiner

Each of claims 4 & 10 recites, "a standard reset gate." Since "standard" can change over time, the metes and bounds of the claim cannot be ideally ascertained.

Reply to the Examiner's Comments

Claim 4 has been cancelled and in Claim 10, "standard " has been deleted.

The following rejection(s) applied to claims 4 & 10 based on best understood in view of the 112 second paragraph rejection above.

Double Patenting

Comments of the Examiner

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman,* 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi,* 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum,* 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel,* 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.32 1(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of U. S. Patent No. 6,580,106 B2 (hereafter, referred as Patent '106). Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of the instant application is encompassed by claims I & 3 of the Patent '106. It should be noted that "a drain" as claimed in the instant application is inherently met by the claimed vertical punch through transistor in the Patent '106 because a drain must exist as a fundamental terminal in addition to a source and gate of the claimed transistor in order for the transistor to function.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller,* 397 F.2d 350, 158 USPQ 210 (CCPA 1968).. See also MIPEP § 804.

Reply to the Examiner' Comments

Applicant is very sorry that confusion in terminology has occurred that led to an impression of double patenting. The US 6,580,106 B2 clearly states that the vertical punch through transistor is used but with a **junction gate surrounding its source and connected to it.** The word "connected to it" clearly means an electrically conductive connection as is clear from the specification. There are many structures and features "physically connected" to the gate such as oxide, substrate, metal wiring, etc. The meaning of the connected is clear to those working in the field and word connected is not used in the sense of physical connectedness in those applications.

Drawing 400 of the patent 106 clearly indicates that no MOS gate is present in the region 320 over the punch-through transistor region. This is the specific and distinct feature of the vertical punch-through structure in 106 that actually led the applicant to file another application. This clearly contrasts with the structure shown in the drawing in FIG.2. of the present application where the gate 204 that surrounds the source 209 and is electrically connected to it. None of the cited art shows this feature and none of the objections based on physical connectedness are therefore relevant.

Claim 7 has been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 in view of the Admitted Prior Art. Note an assumption for a CCD and CMOS device mentioned in section 4 above.

Comments of the Examiner

Regarding claim 7, the Patent '106 claims in claims 1 & 3 an image sensor device comprising CMOS and having all features as claimed in claim 7 of the instant application The claims 1 & 3 of the Patent '106 do not include a CCD. However, as admitted by the Applicant in Fig. 1 and pages 6-8 of the specification that the CCD and CMOS device is a well-known imaging device, having a typical I3CD structure which comprises a. substrate(105) and agate (104) surrounding its source (109).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CMOS device in the Patent '106 to include a CCD structure in an alternative implementation of an imaging device based on a well-known BCD structure.

Reply to the Examiner's Comments

Same as above, it is a distinctly different structure with MOS gate connected to the source not a junction gate connected to the source

Comments of the Examiner

Claim 2 has been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 in view of Kubo Kazuya (JP61-188965).

Comments of the Examiner

Regarding claim 2, the claimed invention of Patent '106 *does not clearly* disclose a charge present under the gate modulates the punch through potential barrier of the vertical charge-sensing punch-through transistor. It is taught by Kubo that a barrier height of a vertical punch through transistor (Fig. 1) is modulated by the charges present under the gate (4, 7) to implant excess charge into substrate 1 for suppressing a blooming, expanding a dynamic range and improving the S/N ratio. See Abstract and Fig. 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of modulating the punch through potential barrier of the vertical charge-sensing punch-through transistor by a charge present under the gate for suppressing a blooming, expanding a dynamic range and improving the S/N ratio.

Reply to the Examiner's Comments

Kubo Kazuya (JP 61-188965) dos not show a vertical punch-through transistor with gate surrounding its source and being connected to it as defined in the specification.

Claims 3, 5, 6, 8, 9, 11 & 12 have been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims I and 3 of the Patent '106 and the Admitted Prior Art and in further view of Kubo Kazuya (JP 6 1-188965).

Comments of the Examiner

Regarding claim 8, the claimed invention of Patent '106 and the Admitted Prior Art do not clearly disclose a charge present under the gate modulates the punch through potential barrier of the vertical charge-sensing punch-through transistor. It is taught by Kubo that a barrier height of a vertical punch through transistor (Fig. 1) is modulated by the charges present under the gate (4, 7) to implant excess charge into substrate 1 for suppressing a blooming, expanding a dynamic range and improving the S/N ratio. See Abstract and Fig. 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of modulating the punch through potential barrier of the vertical charge-sensing punch-through transistor by a charge present under the gate for suppressing a blooming, expanding a dynamic range and improving the S/N ratio.

Regarding claims 3 & 9, the Admitted Prior Art further shows a charge reset means (111, Fig. 1) adjacent to and coupled to the vertical charge-sensing punch-through transistor (it is noted that the transistor originates from the Patent '106) to remove charge therefrom (see first paragraph on page 8 of the specification).

Regarding claims 5 & 11, the Admitted Prior Art further discloses that the charge reset means (111) is a resistive reset gate (see first paragraph on page ~ of the specification).

Regarding claims 6 & 12, the Applicant further admits that the resistive reset gate and a lateral punch-through reset gate are obvious variants over each other as well known in the art (see first paragraph on page 10 of the specification). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the charge reset means by using either a resistive gate or a lateral punch through transistor as an alternative over each other.

Reply to the Examiner's Comments

Claims 3,5,6,8,11,& 12. Claims 4,5,& 6 have been cancelled. In regard to Claims 3, 8, 11 and 12, the same applies as above.

Claims 4 & 10 have been rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims I and 3 of the Patent '106 and the Admitted Prior Art and in further view of Lee et al (US 5,904,493). Note "best understood" mentioned in section 5 above.

Comments of the Examiner

Regarding claims 4 & 10, the claimed invention of Patent '106 and the Admitted Prior Art do not explicitly teach that the charge reset means is a standard reset gate. Lee teaches that it is a design choice for a reset means to be constructed with a standard reset gate (using standard CMOS voltage level) or other reset gates using higher voltage level in a combined CCD and CMOS imaging device (see Lee, col. 3, line *65* — col. 4, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art to construct the charge reset means by using a standard reset gate as one of design choices for the charge reset means.

Reply to the Examiner's Comments

Lee does not show any structure similar to present invention of a MOS gate surrounding the source and being connected to it.
Claim Rejections -35 USC § 103

11. Claims 1-3, *5-9*, 11 & 12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art in view of Kubo Kazuya (JP 61-188965).

Comments of the Examiner

Regarding claim 1, the Admitted Prior Art (Fig. 1) discloses a charge detection device for use in an image sensor, the charge detection device including airansistor (at Vs, Fig. 1) having a source (109), drain (108, 111) and gate (104), said transistor having the gate surrounding the source and connected to it (see the paragraph starting from page 6 to page 8 of the specification). It is noted that "connected" is considered as physically connected, not necessary to be electrically connected.

The Admitted Prior Art does not teach that the transistor is a vertical punch-through transistor. However, as taught by Kubo, a vertical punch-through occurs between the source region 3 and substrate 1 of a transistor so that excess charges are implanted into the substrate I to suppress a blooming, to expand a dynamic range and to improve S/N ratio by removing excess charges after photoelectric converting (see Abstract and Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the Admitted Prior Art to include the teaching of Kubo for a vertical punch-through transistor so as to suppress a blooming, to expand a dynamic range and to improve S/N ratio by removing excess charges after photoelectric converting, thereby the image quality would be improved.

Regarding claim 2, it is clear from Kubo' s teaching that the barrier height of the vertical punch through transistor (Fig. 1) is modulated by the charges present under the gate (4, 7). See Abstract.

Regarding claim 3, it is further disclosed by Admitted Prior Art that a charge reset means (111, Fig. 1) adjacent to and coupled to the vertical charge-sensing punch-through transistor to remove charge therefrom (see first paragraph on page 8 of the specification).

Regarding claim 5, the Admitted Prior Art discloses that the charge reset means (111) is a resistive reset gate (see first paragraph on page 8 of the specification).

Regarding claim 6, the Applicant further admits that the resistive reset gate and a lateral punch-through reset gate are obvious variants over each other as well known in the art (see first paragraph on page 10 of the specification). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the charge reset means by using either a resistive gate Or a lateral punch through transistor as an alternative over each other.

Regarding claim 7, see the analysis of claim 1 in section 10. The Admitted Prior Art discloses an imaging device in form of a BCD structure that is also a CCD and CMOS device (see Fig. 1 and pages 6-8 in the specification).

Regarding claims 8 & 9, see the analyses of claims 2 & 3, respectively, in section 11.

Regarding claims 11 & 12, see the analyses of claims 5 & 6, respectively, in section 11.

Reply to the Examiner's Comments

In regard to Claims 1-3, 5-9,11 & 12, the prior art shows a gate surrounding the source, but the gate is not connected to source. The source 109 and gate 104 have separate terminals. The connected means electrically, conductively connected as is clear from the specification.

Claims 4 & 10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art and Kubo Kazuya as applied to claims 1 & 7 and in further view of Lee et al.(US 5,904,493).

Comments of the Examiner

Regarding claims 4 & 10, the Admitted Prior Art and Kubo do not explicitly teach that the charge reset means is a standard reset gate. Lee teaches that it is a design choice for a reset means to be constructed with a standard reset gate (using standard CMOS voltage level) or other reset gates using higher voltage level in a combined CCD and CMOS imaging device (see Lee, col. 3, line 65 — col. 4, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art to construct the charge reset means by using a standard reset gate as one ,of design choices for the charge reset means.

Reply to the Examiner's Comments

As explained above Prior art of Kubo is not relevant to this application since it does not show anywhere the gate being electrically connected to source. The art of Lee is not relevant since does not show any vertical structure and the reset means claims have been dropped from the application.

To prevent the confusion in terminology the claims have been modified to include the word "conductively connected" to...

Summary

Since the claims have been amended to overcome the rejection of the Examiner, and new claims 13-16 have been added, it is respectively requested that the claim as amended be allowed and the application passed to issue.

Respectively submitted,

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